AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A pixel sensor comprising:

an n-type photosensitive element for converting an optical image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a readout circuit coupled to said source follower transistor and comprising a p-type transistor; and

a first reset circuit configured to provide a reset signal at said gate of said source follower transistor, where said first reset circuit includes at least one p-type transistor having a gate for receiving a first and a second control signal thereat to control a reset operation of said photosensitive element.

2. (Original) The pixel sensor of claim 1, wherein said p-type transistors are MOSFET p-type transistors.

3. (Original) The pixel sensor of claim 1, wherein said n-type photosensitive element is an n-type photodiode.

4. (Original) The pixel sensor of claim 3, wherein said n-type photodiode is formed in a square layout design.

5. (Original) The pixel sensor of claim 3, wherein said n-type photodiode is formed in a circular layout design.

6. (Previously Presented) The pixel sensor of claim 1, further comprising:

a p-type substrate in which said n-type photosensitive element is formed.

7. (Original) The pixel sensor of claim 6, further comprising:

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings adapted for connection to a ground voltage, and operating to reduce a leakage current from said n-type photosensitive element.

8. (Previously Presented) The pixel sensor of claim 6, further comprising:

an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent charges from escaping the pixel sensor.

9. (Currently Amended) The pixel sensor of claim 1, further comprising:

a second reset circuit having a p-type MOSFET transistor ~~coupled to an input of said first reset circuit,~~ configured to apply said second control signal to said gate of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

10. (Currently Amended) An image sensing device, comprising:

a p-type substrate;

an n-type photodiode formed in said p-type substrate, where said n-type photodiode operates to convert an optical image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset circuit configured to provide a reset signal for said electrical signal, said first reset circuit including a p-type MOSFET transistor having a gate for receiving a first and a second control signal thereat to control a reset operation of said photodiode; and

a readout circuit operating to buffer said electrical signal, said readout circuit including a p-type MOSFET transistor.

11. (Original) The device of claim 10, further comprising:

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photodiode, said pair of guard rings adapted for connection to a ground voltage, and operating to reduce a leakage current from said n-type photodiode.

12. (Original) The device of claim 11, further comprising:

an n-type well provided adjacent to one of said pair of p+ type guard rings, said n-type well adapted for connection to a supply voltage, and operating to prevent crosstalk between pixels in the image sensing device.

13. (Currently Amended) The device of claim 10, further comprising:

a second reset circuit having a p-type MOSFET transistor ~~coupled to an input of said first reset circuit,~~ configured to apply said second control signal to said gate of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

14. (Currently Amended) A CMOS image sensor system, comprising:

an array of active pixel sensors, each pixel sensor of said array including:

an n-type photosensitive element operating to convert an optical image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a pixel readout circuit, where said pixel readout circuit includes at least one p-type transistor coupled to receive an output of said source follower transistor;

a first reset circuit configured to provide a reset level for a pixel output signal, where said first reset circuit includes at least one p-type transistor having a gate for receiving a first and a second control signal thereat to control a reset operation of said photosensitive element;

a control circuit configured to provide timing and control signals to enable read out of data stored in said array of active pixel sensors; and

a column readout circuit operating to receive and process said data stored in said array of active pixel sensors.

15. (Previously Presented) The CMOS image sensor of claim 14, further comprising:

a p-type substrate in which said array of pixel sensors is formed.

16. (Previously Presented) The CMOS image sensor of claim 15, each pixel sensor further comprising:

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings adapted for connection to a ground voltage, and operating to reduce a leakage current from said n-type photosensitive element.

17. (Currently Amended) The CMOS image sensor of claim [[15]] 16, each pixel sensor further comprising:

an n-type well provided adjacent to at least one of said pair of p+ type guard rings, said n-type well adapted for connection to a supply voltage, and operating to prevent crosstalk between pixels.

18. (Currently Amended) The CMOS image sensor of claim 14, each pixel sensor further comprising:

a second reset circuit having a p-type MOSFET transistor ~~coupled to an input of said first reset circuit,~~ configured to apply said second control signal to said gate of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation.

19. (Previously Presented) The pixel sensor of claim 1, wherein the p-type transistor of the readout circuit comprises a row select transistor for selectively reading out said pixel output signal.

20. (Previously Presented) The pixel sensor of claim 19, wherein said row select transistor is coupled to receive an output of said source follower transistor.

21. (Previously Presented) The device of claim 10, wherein the device is a CMOS image sensing device and said p-type transistors provide radiation hardness without any radiation protective enclosure.

22. (Previously Presented) The device of claim 10, wherein said source follower transistor is a p-type MOSFET transistor.

23. (Previously Presented) The device of claim 10, wherein the readout circuit comprises a row select transistor for selectively outputting said pixel output signal.

24. (Previously Presented) The device of claim 23, wherein said row select transistor is coupled to receive an output of said source follower transistor.

25. (Previously Presented) The CMOS image sensor of claim 14, wherein said readout circuit includes a row select transistor for selectively connecting the pixel sensor to a column line of the array.

26. (Previously Presented) The CMOS image sensor of claim 25, wherein said row select transistor is coupled to receive said output of said source follower transistor.

27. (Previously Presented) The CMOS image sensor of claim 14, wherein said p-type transistors provide radiation hardness to the array of active pixel sensors.

28. (Currently Amended) An array of pixel sensors comprising:

a plurality of pixels formed in a p-type substrate, at least one of said pixels comprising:

an n-type photodiode formed in said substrate and for generating an electrical signal in response to an applied optical image;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset circuit coupled to said gate and responsive to a first reset control signal for providing a global reset value as said pixel output signal;

a second reset circuit coupled to an input of said first reset circuit and ~~responsive to~~ for generating a second reset control signal for operating said first reset circuit to allow a pixel-by-pixel reset;

a p-type row select transistor for selectively connecting the pixel to an associated column line of the array for readout of the pixel output signal; and

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings located on either side of said n-type photodiode.

29. (Previously Presented) The array of pixel sensors of claim 28, said at least one pixel further comprising an n-type well located adjacent at least one of said pair of p+ type guard rings in said p-type substrate.

30. (Previously Presented) The array of pixel sensors of claim 28, wherein said p-type transistors provide said at least one pixel with radiation hardness, without a radiation protective enclosure.

31. (New) An array of pixel sensors comprising a plurality of pixel sensors arraigned in a plurality of rows and columns, each pixel sensor comprising:

an n-type photosensitive element for converting an optical image to an electrical signal;

a p-type source follower transistor for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset transistor having a first reset gate configured to receive a first reset control signal for performing a reset operation for said photosensitive element, said first reset control signal being commonly applied to a row of pixels; and

a second reset transistor having a second reset gate configured to receive a second reset control signal for performing a reset operation for the photosensitive element as an individual pixel reset.

32. (New) The pixel array of claim 31, wherein the first and second reset transistors are p-type MOSFET transistors.

33. (New) The pixel array of claim 31, each pixel cell further comprising:

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element, said pair of guard rings adapted for connection to a ground voltage, and operating to reduce a leakage current from said n-type photosensitive element.